IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A multi-chip module ~~as defined in claim 2~~including semiconductor devices and a wiring substrate for mounting the semiconductor devices, wherein

the wiring substrate comprises a first substrate having through holes, a first wiring layer formed on one surface of the first substrate and having first wirings and a first insulation layer, a second wiring layer formed on the other surface of the first substrate and having second wirings and a second insulation layer, in which the heat expansion coefficient is different between the first wiring layer and the second wiring layer, wherein

the heat expansion coefficient of the first wiring layer is close to the heat expansion coefficient of the semiconductor device, and the heat expansion coefficient of the second wiring layer is close to the heat expansion coefficient of a mounting substrate for mounting the wiring substrate.

3. (Original) A multi-chip module having semiconductor devices and a wiring substrate for mounting the semiconductor devices, wherein

the wiring substrate comprises:

a first substrate having through holes;

a first wiring layer having first wirings and a first insulation layer formed to the surface of the first substrate on the side where the semiconductor devices are mounted; and

a second wiring layer having second wirings and a second insulation layer formed to the surface of the first substrate on the side where the wiring substrate is mounted;

wherein the heat expansion coefficient of the first wiring layer is close to the heat expansion coefficient of the semiconductor device, and the heat expansion coefficient of the second wiring layer is close to the heat expansion coefficient of a mounting substrate for mounting the wiring substrate.

4. (Previously Presented) A multi-chip module according to claim 3, wherein:

said first substrate includes through holes with a heat expansion coefficient being from 3 ppm/°C to 5 ppm/°C;

a third insulation layer is formed to the surface of the second wiring layer on the side opposite to the first substrate; and

wherein the modulus of elasticity of the third insulation layer is from 0.1 GPa to 10 GPa.

5. (Previously Presented) A multi-chip module according to claim 3, wherein:

said first substrate includes through holes with a heat expansion coefficient being from 3 ppm/°C to 5 ppm/°C;

a third insulation layer is formed to the surface of the second wiring layer on the side opposite to the first substrate; and

wherein the third insulation layer relieves the thermal stresses caused between the wiring substrate and a mounting substrate for mounting the wiring substrate.

6. (Original) A multi-chip module as defined in claim 4, wherein the first substrate is a glass substrate.

7. (Original) A multi-chip module as defined in claim 5, wherein the first substrate is a glass substrate.

8. (Original) A multi-chip module as defined in claim 4, wherein the third insulation layer is formed on a region with no opening of a hole formed in the first substrate.

9. (Original) A multi-chip module as defined in claim 5, wherein the third insulation layer is formed on a region with no opening of a hole formed in the first substrate.

10. (Original) A multi-chip module as defined in claim 4, wherein the heat expansion coefficient of the third insulation layer is from 3 ppm/°C to 300 ppm/°C.

11. (Original) A multi-chip module as defined in claim 5, wherein the heat expansion coefficient of the third insulation layer is from 3 ppm/°C to 300 ppm/°C.

12. (Original) A multi-chip module as defined in claim 4, wherein the thickness of the third insulation layer is from 30 μm to 250 μm.

13. (Original) A multi-chip module as defined in claim 5, wherein the thickness of the third insulation layer is from 30 μm to 250 μm.

14. (Original) A multi-chip module as defined in claim 4, wherein the third insulation layer comprises a resin having imide bondings.

15. (Original) A multi-chip module as defined in claim 5, wherein the third insulation layer is formed by printing using a mask.

16. (Original) A multi-chip module as defined in claim 5, wherein the third insulation layer is formed by printing using a mask.

17. (Original) A multi-chip module as defined in claim 4, wherein the through holes in the first substrate are formed by sand blasting.

18. (Original) A multi-chip module as defined in claim 5, wherein the through holes in the first substrate are formed by sand blasting.

19. (Original) A multi-chip module as defined in claim 17, wherein the semiconductor device is mounted on the surface where the opening diameter of the first through hole is smaller.

20. (Original) A multi-chip module as defined in claim 18, wherein the semiconductor device is mounted on the surface where the opening diameter of the first through hole is smaller.